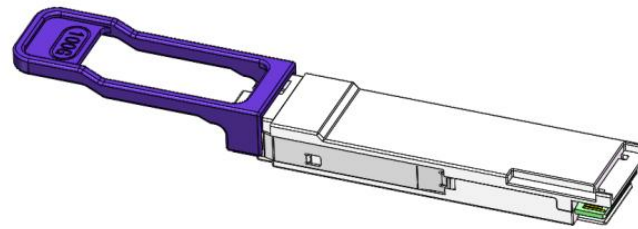
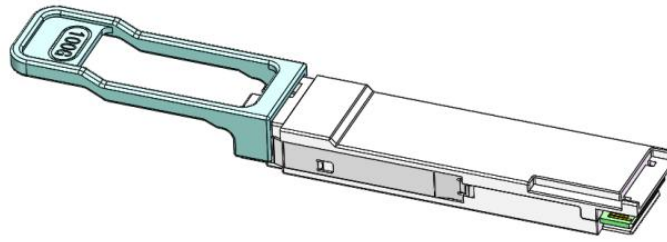


Product Specification Sheet

RoHS Compliant 100Gb/s QSFP28 BIDI 40km Optical Transceiver



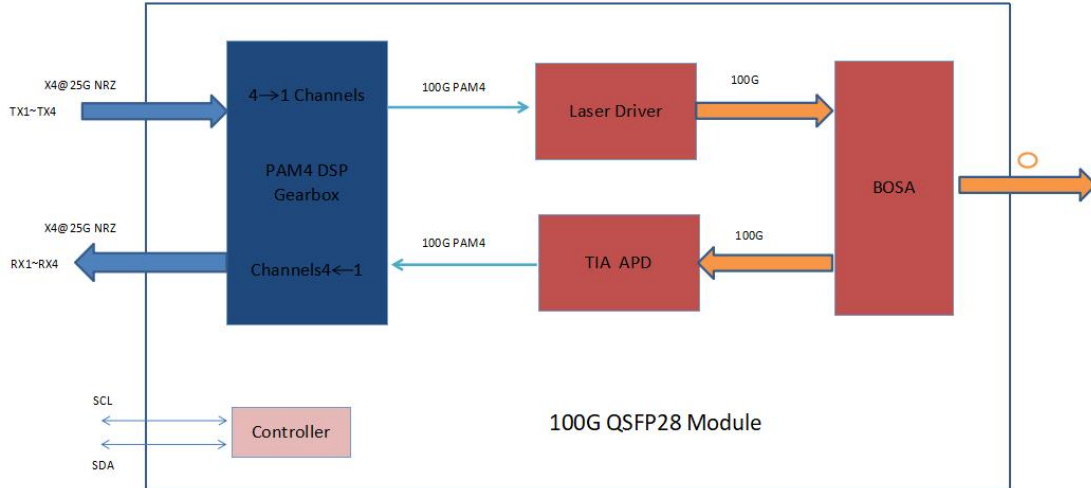
Product Features

- Simplex LC receptacle optical interface
- Single +3.3V power supply
- Up to 40km transmission on SMF
- EML laser and APD receiver
- Hot-pluggable QSFP28 MSA form factor
- Lane signaling rate 53.125GBd with PAM4
- Low power dissipation(Max:4.5W)
- Built in digital diagnostic function
- Operating case temperature range:0°C to 70°C
- Compliant with IEEE 802.3bs and 100G Lambda MSA
- I2C Communication Interface

Applications

- 100GBASE-ER1-40 BIDI
- Transmission up to 40km

Functional Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	V _{cc}	-0.5	4	V	
Storage Temperature	T _s	-40	85	°C	
Relative Humidity	R _H	0	85	%	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Data Rate(Electrical)	DR		25.78	26.5625	Gb/s	CAUI-4
Data Rate(Optical)	DR		106.25		Gb/s	
Supply Voltage	V _{cc}	3.14	3.3	3.47	V	
Supply Current	I _{cc}			1.36	A	
Operating Case Temp.	T _c	0		70	°C	

Electrical Characteristics (T_{op}=0~70°C, V_{cc}=3.14~3.47V)

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Signaling rate	Rate		25.78			Gbps
Differential data input swing	V _{in,pp}	100		900	mV	
Differential termination mismatch	T _m			10	%	
Receiver						
Signaling rate	Rate		25.78			Gbps
Differential data output swing	V _{out,pp}	100		900	mV	
Differential termination mismatch	T _m			10	%	
Transition time, 20% to 80%	Tr,Tf	9.5			ps	
Vertical Eye Closure	VEC			6.5	dB	
Eye width at 10-15robability	EW15	0.57			UI	
Eye height at 10-15probability	EH15	228			mV	

Optical Characteristics (T_{op}=0~70°C, V_{cc}=3.14~3.47V)

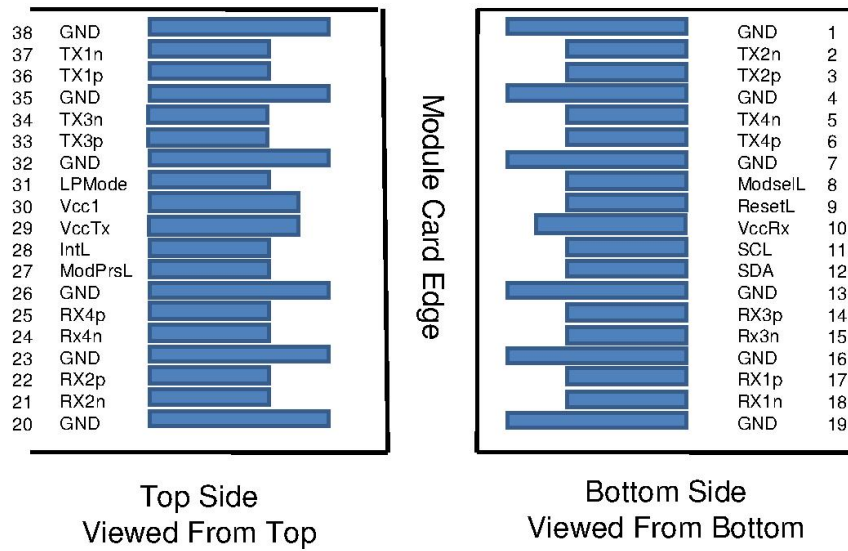
(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate		GBd		53.125		
Lane Wavelength Range	$\lambda 1$	nm	1303.54	1304.58	1305.63	
	$\lambda 2$	nm	1308.09	1309.14	1310.19	
Average launch power	P _{avg}	dBm	1.7		7.1	1
Outer Optical Modulation Amplitude (OMA _{outer})	P _{OMA1}	dBm	4.7		7.9	
Outer Optical Modulation Amplitude (OMA _{outer}) (min) for 1.4 dB ≤ TDECQ ≤ TDECQ (max)	P _{OMA2}	dBm	3.3+TDECQ			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) (max)	TDECQ	dB			3.9	
Extinction ratio	ER	dB	5			
Side-mode suppression ratio	SMSR	dB	30			
Average launch power of OFF transmitter (max)	P _{OFF}	dBm			-15	
Transmitter Reflectance	RL				-26	2
Receiver						
Receive Rate		GBd		53.125		
Lane Wavelength Range	$\lambda 1$	nm	1308.09	1309.14	1310.19	
	$\lambda 2$	nm	1303.54	1304.58	1305.63	
Overload Input Optical Power	P _{max}	dBm	-2.4			3
Average Receive Power	P _{in}	dBm	-16		-3.4	4
Receiver sensitivity (OMA _{outer}) (max) For TECQ < 1.4 dB For 1.4 ≤ TECQ 3.6 dB For 1.4 ≤ TECOS 3.9 dB	P _{sens1}	dBm			13.8 -15.2 + TECO	5
Return Loss	RL	dB	-26			
Los De-Assert	P _d	dBm			-16	
Los Assert	P _a	dBm	-30			

Notes:

- 1、Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
- 2、Transmitter Reflectance is defined looking into the transmitter.
- 3、The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane.
- 4、Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
- 5、CAUI4 mode, the Pre-FEC BER level is 2E-4.

Pin Description



Pin	Name	Logic	Description	
1	GND		Ground	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	10
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	10
4	GND		Ground	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	10
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	10
7	GND		Ground	1
8	ModSelL	LVTTL-I	Module Select	3
9	ResetL	LVTTL-I	Module Reset	4
10	Vcc Rx		+3.3V Power Supply Receiver	2
11	SCL	LVC MOS	2-wire serial interface clock	5
12	SDA	LVC MOS	2-wire serial interface data	5
13	GND		Ground	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	9
15	Rx3n	CML-O	Receiver Inverted Data Output	9
16	GND		Ground	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	9
18	Rx1n	CML-O	Receiver Inverted Data Output	9
19	GND		Ground	1
20	GND		Ground	1
21	Rx2n	CML-O	Receiver Inverted Data Output	9
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	9
23	GND		Ground	1
24	Rx4n	CML-O	Receiver Inverted Data Output	9
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	9
26	GND		Ground	1
27	ModPrsL	LVTTL-O	Module Present	6
28	IntL	LVTTL-O	Interrupt	7
29	Vcc Tx		+3.3V Power supply transmitter	2
30	Vcc1		+3.3V Power supply	2
31	LPMODE	LVTTL-I	Low Power Mode	8
32	GND		Ground	1

33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	10
34	Tx3n	CML-I	Transmitter Inverted Data Input	10
35	GND		Ground	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data	
37	Tx1n	CML-I	Transmitter Inverted Data Input	10
38	GND		Ground	1

Notes:

1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA. Recommended host board power supply filtering is shown below .

3: The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4: The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

5: Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1.

Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology.

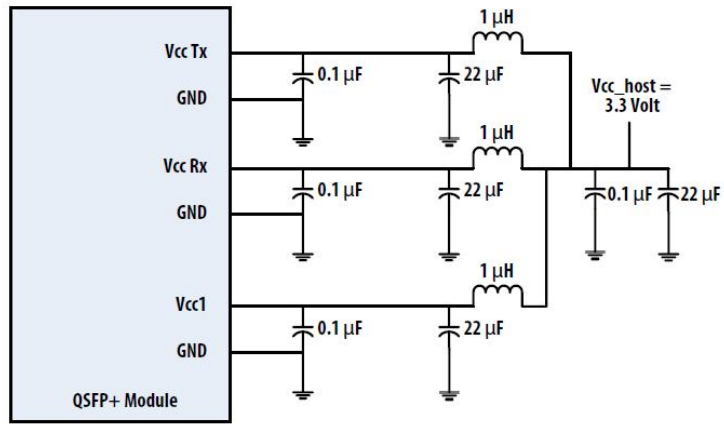
6: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

7: IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

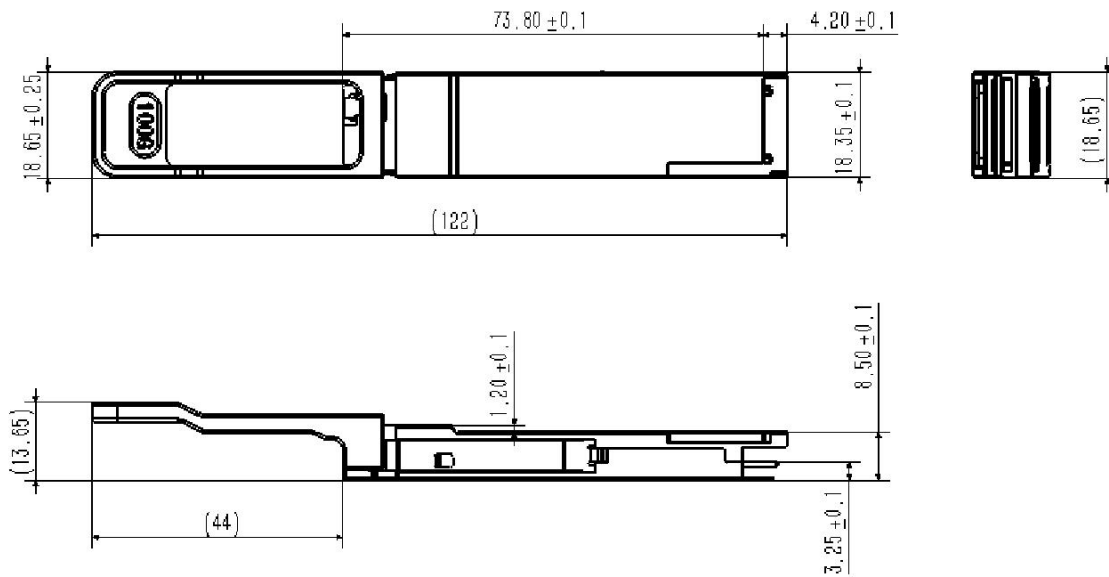
8: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control

used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

Recommended Power Supply Filter



Package Dimensions



Ordering Information

Part Number	Description
FBL-QSFP28-100G-BX40-D	100G QSFP28 BIDI T1304R1309 40km, 0~70°C, with Digital Diagnostic Monitor
FBL-QSFP28-100G-BX40-D	100G QSFP28 BIDI T1309R1304 40km, 0~70°C, with Digital Diagnostic Monitor

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